

Back

6,525,720

# 8

(12) UK Patent Application (19) GB (11) 2 368 445 (13) A

(43) Date of A Publication 01.05.2002

(21) Application No 0112233.2

(22) Date of Filing 18.05.2001

(30) Priority Data

(31) 00038469

(32) 06.07.2000

(33) KR

(51) INT CL<sup>7</sup>

G09G 3/36

(52) UK CL (Edition T )

G5C CA342 CHBH

(56) Documents Cited

JP 100319916 A

JP 090191435 A

US 6069619 A

US 5757365 A

(71) Applicant(s)

LG Philips LCD Co Ltd

(Incorporated in the Republic of Korea)

20 Yoido-dong, Youngdungopo-ku, Seoul,  
Republic of Korea

(58) Field of Search

UK CL (Edition T ) G5C CHBH CHBM

INT CL<sup>7</sup> G09G 3/36

ONLINE DATABASE: EPODOC, JAPIO, WPI

(72) Inventor(s)

Jong Sang Baek

(74) Agent and/or Address for Service

Edward Evans Barker

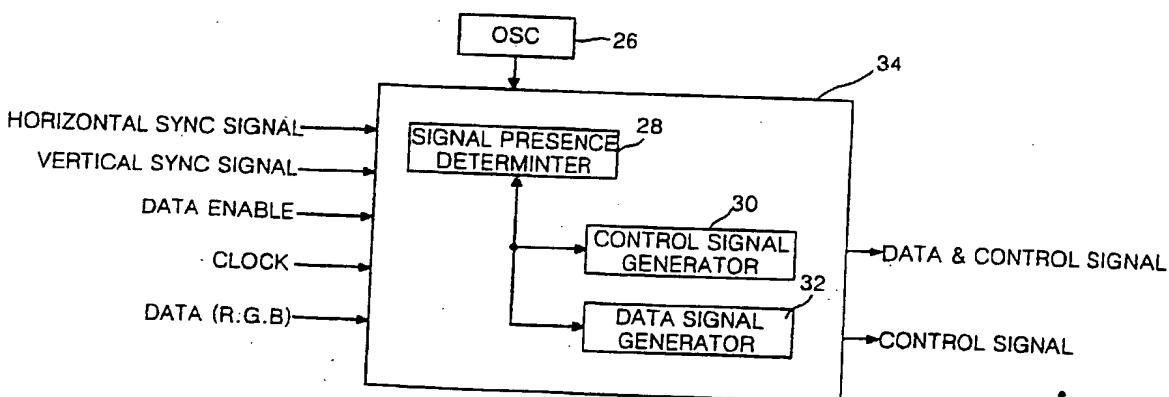
Clifford's Inn, Fetter Lane, LONDON, EC4A 1BZ,  
United Kingdom

(54) Abstract Title

Liquid crystal display and driving method thereof

(57) A liquid crystal display device is adapted to display certain information to a user when no signal is input after power was applied to the liquid crystal display device. In the device, a liquid crystal display panel has pixel electrodes arranged in a matrix. A timing controller 34 generates and outputs control signals for driving the liquid crystal display panel in response to a timing synchronizing signal inputted from the exterior thereof, and the timing controller to display a data inputted from the timing controller on the liquid crystal display panel in response to the control signal. An oscillator 26 generates a pre-synchronizing signal having a desired frequency to apply the same to the timing controller 34. A signal presence determiner 28 compares the timing synchronizing signal with the pre-synchronizing signal to generate a determining signal indicating an input existence of the timing synchronizing signal. A control signal generator 30 generates a control signal on the basis of the pre-synchronizing signal in response to a determining signal indicating no input of the timing synchronizing signal. A data storage device stores a certain picture data and outputs the picture data to the drive circuit in response to the determining signal indicating no input of the timing synchronizing signal.

FIG. 3



GB 2 368 445 A

FIG. 1  
PRIOR ART

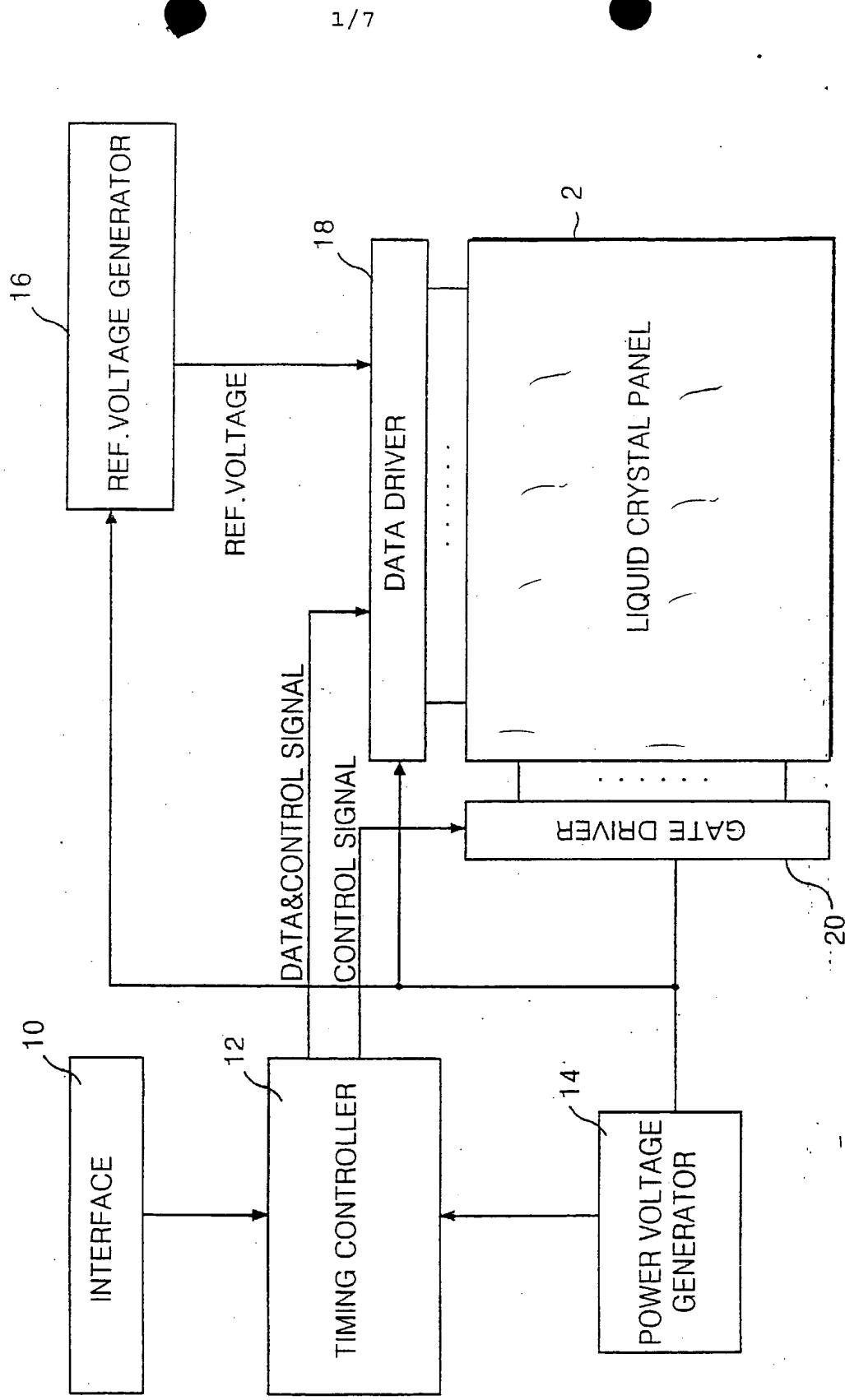


FIG. 2  
PRIOR ART

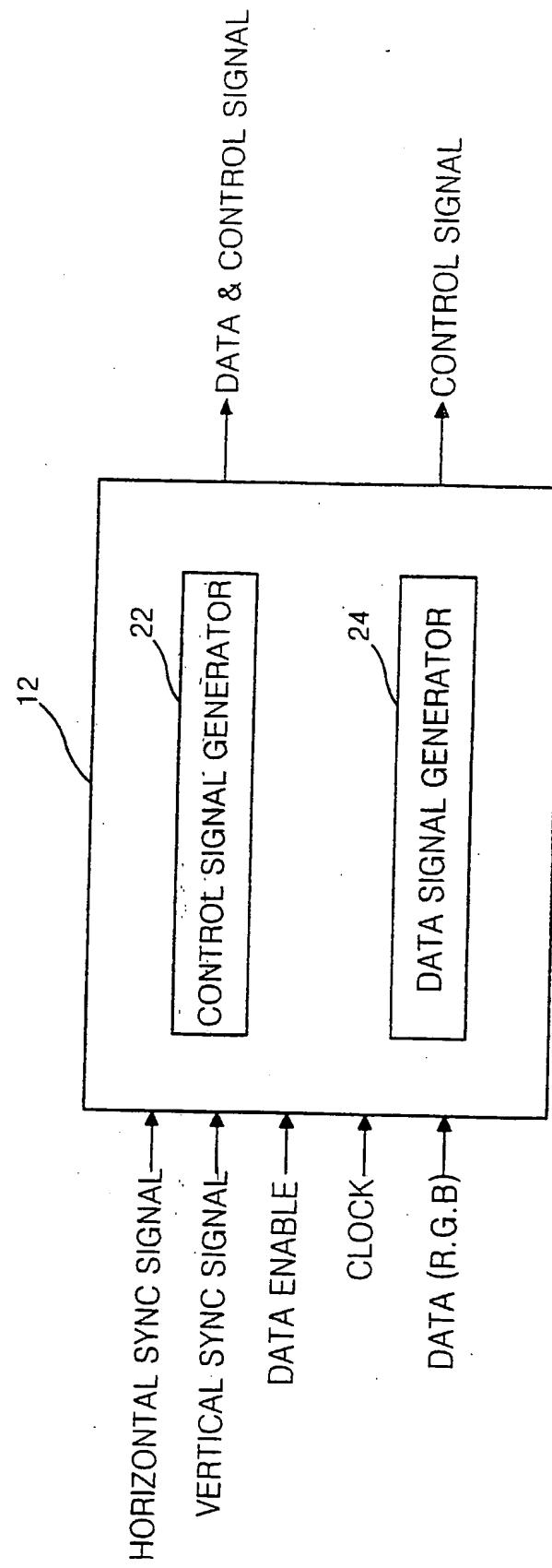


FIG.3

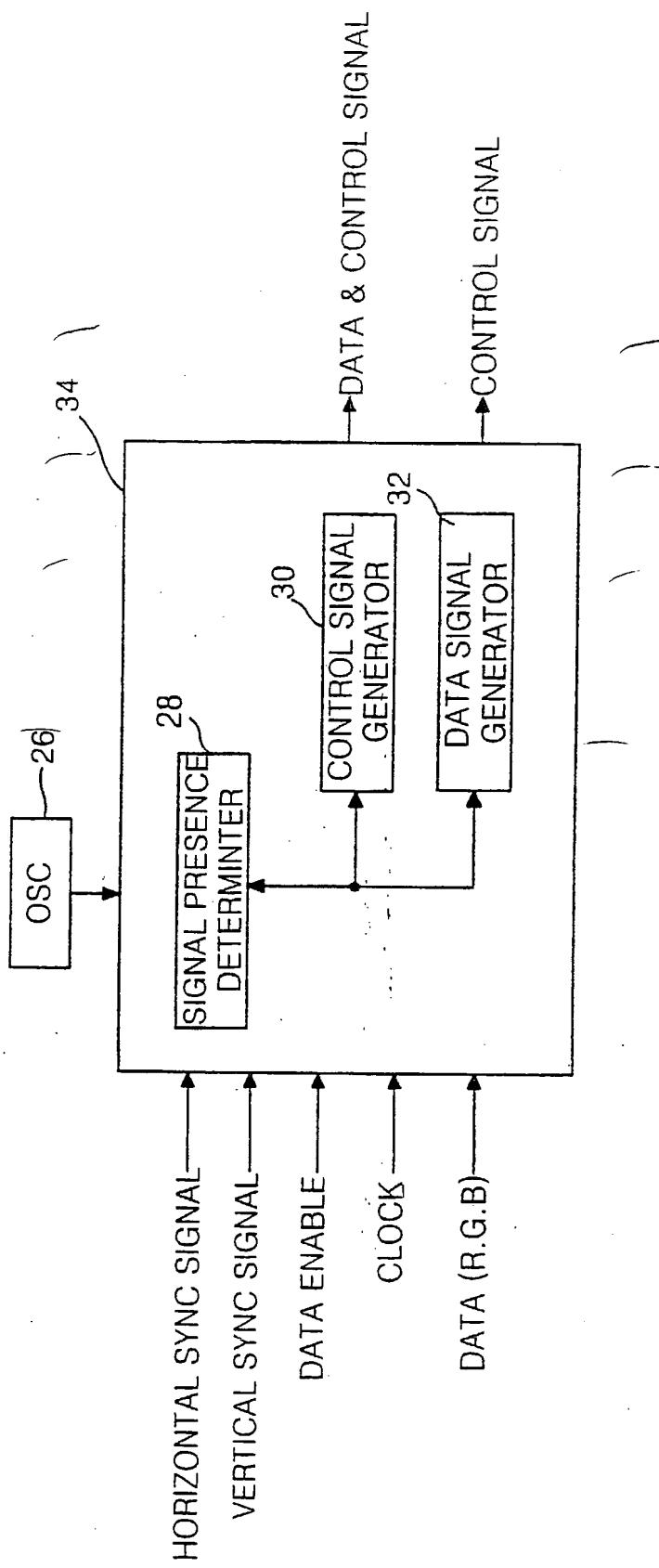


FIG. 4

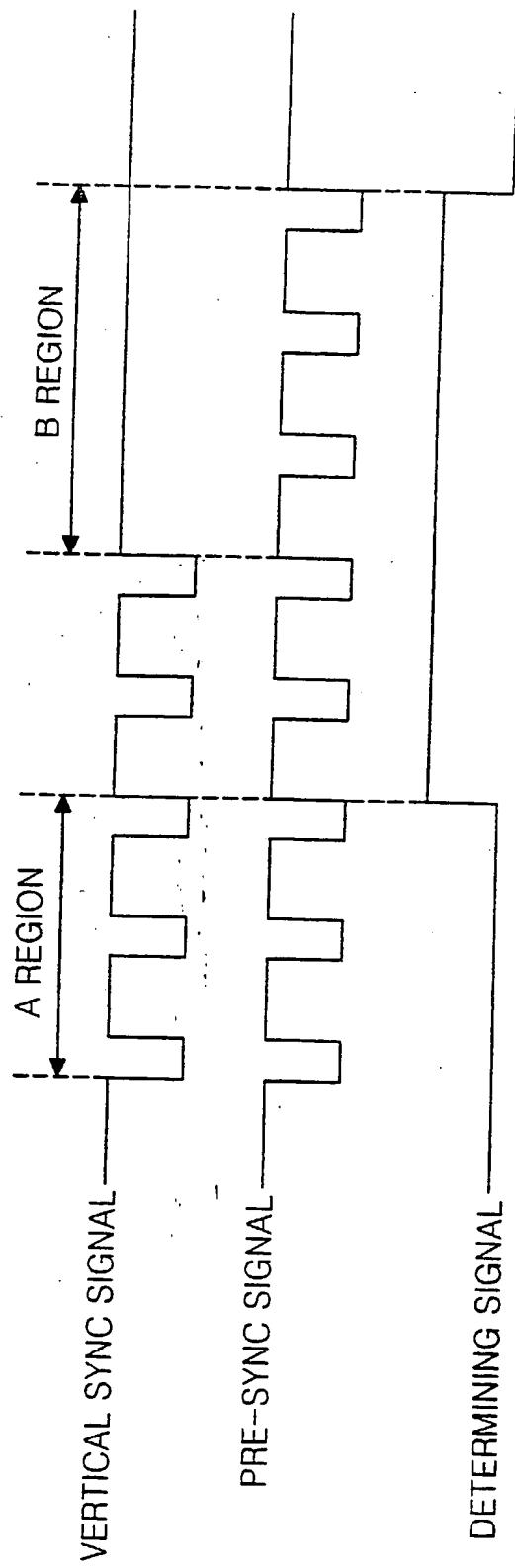


FIG. 5

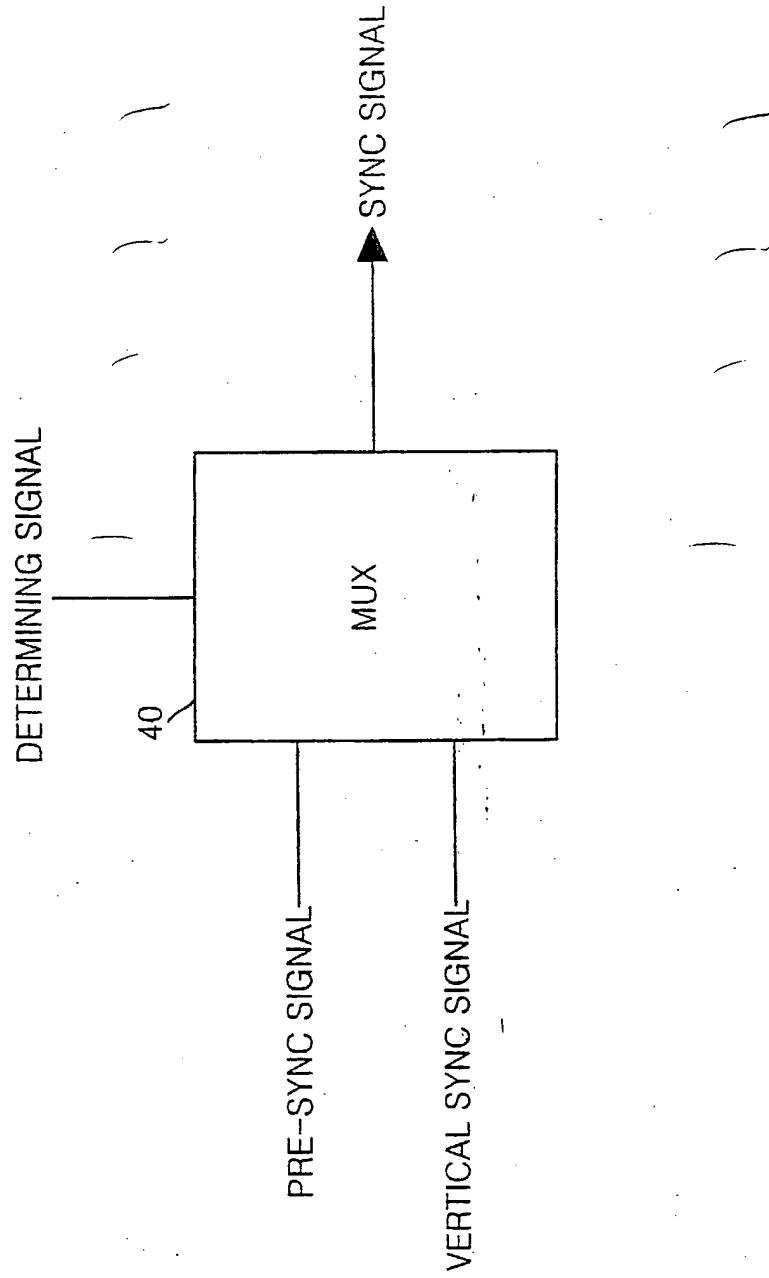


FIG. 6A

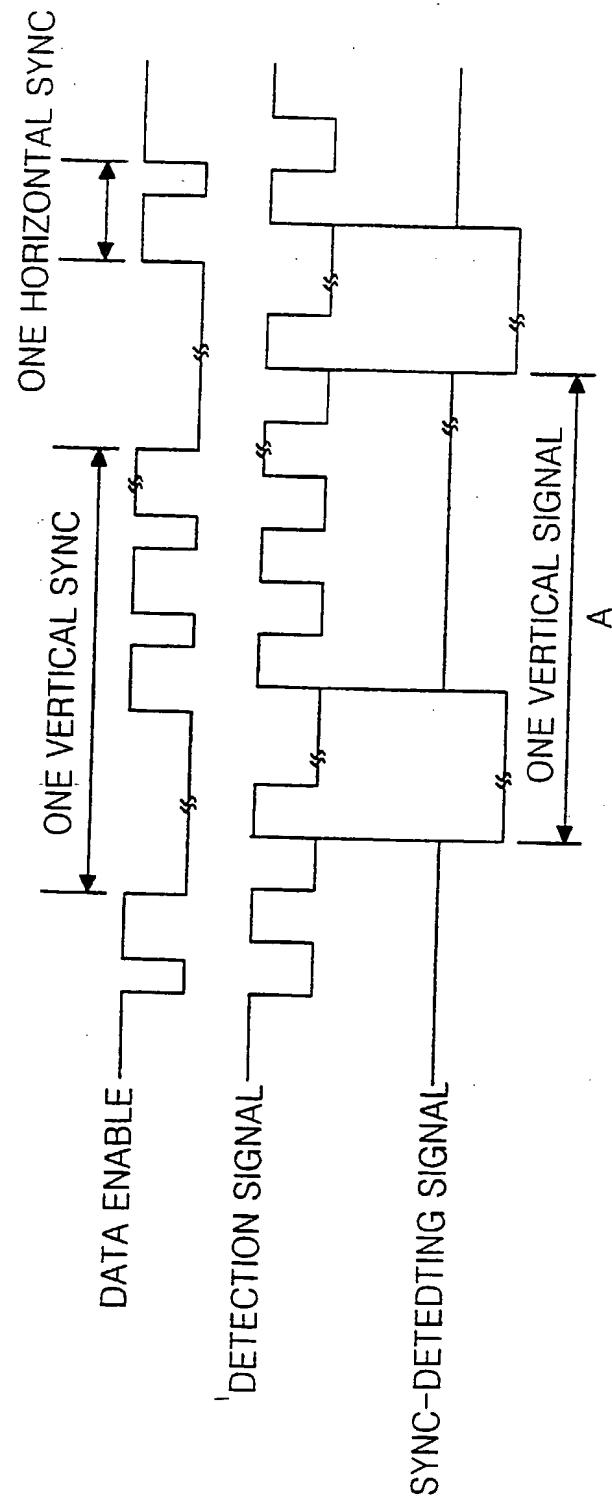
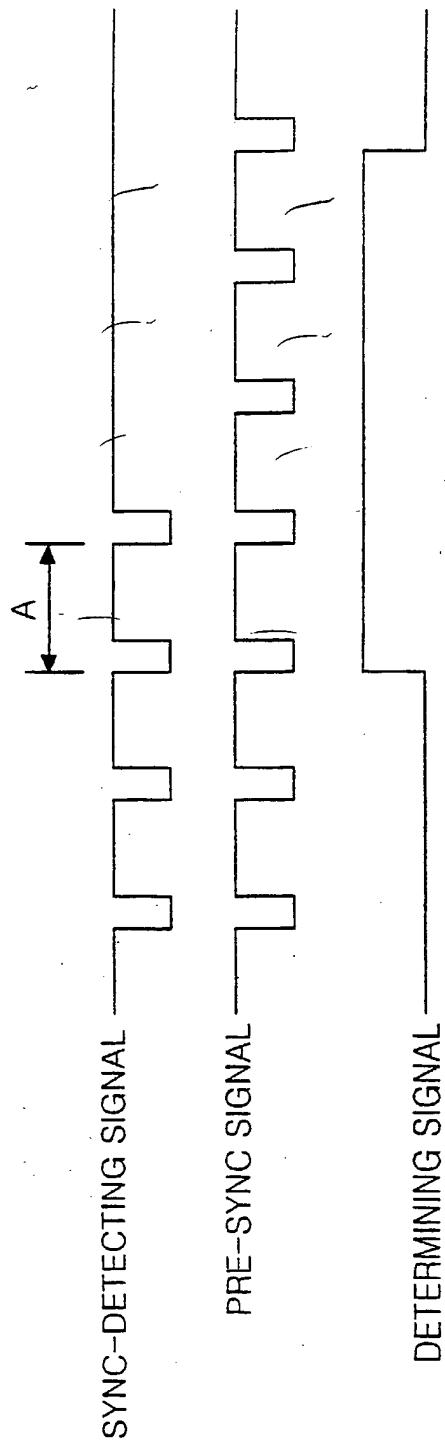


FIG. 6B



## LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

This invention relates to a liquid crystal display, and more particularly to a liquid crystal display device and a driving method thereof that are adapted to display a certain information to a user when no signal is input after a power was applied to the liquid crystal display device.

15

Generally, a liquid crystal display (LCD) has been employed a notebook PC, an office automation equipment and an audio/video equipment, etc. owing to advantages of a small dimension, a thin thickness and a low power consumption. In particular, an active matrix liquid crystal display using thin film transistors (TFT's) as switching devices is suitable for displaying a dynamic image.

25

Fig. 1 is a block diagram showing a configuration of the conventional LCD. In Fig. 1, an interface part 10 receives a data (RGB data) and control signals (e.g., an input clock, a horizontal synchronizing signal, a vertical synchronizing signal and a data enable signal) inputted from a driving system such as a personal computer (not shown) to apply them to a timing controller 12. A low voltage differential signal (LVDS) interface and a

transistor transistor logic (TTL) interface are largely used for a data and control signal transmission to the driving system. Such interfaces may be integrated into a single chip along with the timing controller 12 by 5 collecting each function of them.

The timing controller 12 takes advantages of a control signal inputted via the interface 10 to produce control signals for driving a data driver 18 consisting of a plurality of drive IC's (not shown) and a gate driver 20 consisting of a plurality of gate drive IC's (not shown). 10 Also, the timing controller 12 transfers a data inputted from the interface 10 to the data driver 18. A reference voltage generator 16 generates reference voltages of a digital to analog converter (DAC) used in the data driver 18, which are established by a producer on a basis of a transmissivity to voltage characteristic of the panel. The data driver 18 selects reference voltages of an input data 15 in response to control signals from the timing controller 12 and applies the selected reference voltage to the liquid crystal display panel 2, thereby controlling a rotation angle of the liquid crystal. The gate driver 20 makes an on/off control of the thin film transistors (TFT's) arranged on the liquid crystal panel 22 in 20 response to the control signals inputted from the timing controller 12. Also, the gate driver 20 allows the analog image signals from the data driver 18 to be applied to each pixel connected to each TFT. A power voltage generator 14 supplies an operation voltage to each element, 25 and generates a common electrode voltage and applies it to the liquid crystal panel 22. 30

Fig. 2 is a schematic block diagram showing a

configuration of the timing controller in Fig. 1. In Fig. 2, the timing controller 12 includes a control signal generator 22 and a data signal generator 24. The timing controller 12 receives a horizontal synchronizing signal, a vertical synchronizing signal, a data enable signal, a clock and a data (R,G,B). The vertical synchronizing signal represents a time required for displaying one frame field. The horizontal synchronizing signal represents a time required for displaying one line of the field. Thus, the horizontal synchronizing signal includes pulses corresponding to the number of pixels included in one line. The data enable signal represents a time supplying the pixel with a data.

15 The data signal generator 24 rearranges a data so that desired bits of data (R,G,B) inputted from the interface 10 can be supplied to the data driver 18. The control signal generator 22 receives the horizontal synchronizing signal, the vertical synchronizing signal, the data enable signal and the clock signal to generate various control signals and apply them to the data driver 18 and the gate driver 20. The control signals required for the data driver 18 and the gate driver 20 will be described below. Herein, the control signals used commonly other than the 25 control signals required specially will be described.

The control signals required for the data driver 18 include source sampling clock (SSC), source output enable (SOE), source start pulse (SSP) and liquid crystal 30 polarity reverse (POL) signals, etc. The SSC signal is used as a sampling clock for latching a data in the data driver 18, and which determines a drive frequency of the data drive IC. The SOE signal transfer a data latched by

the SSC signal to the liquid crystal panel. The SSP signal is a signal notifying a latch or sampling initiation of the data during one horizontal synchronous period. The POL signal is a signal notifying the positive or negative 5 polarity of the liquid crystal for the purpose of making an inversion driving of the liquid crystal.

The control signals required for the gate driver 20 include gate shift clock (GSC), gate output enable (GOE) 10 and gate start pulse (GSP) signals, etc. The GSC signal is a signal determining a time when a gate of the TFT is turned on or off. The GOE signal is a signal controlling an output of the gate driver 20. The GSP signal is a signal notifying a first drive line of the field in one 15 vertical synchronizing signal.

The control signals inputted to the data driver 18 and the gate driver 20 as mentioned above are generated by the control signals inputted from the interface 10. Thus, if 20 no control signal is input from the interface 10, then the timing controller 12 fails to generate a control signal. In other words, if any control signals are not inputted from the interface 10 in a power-on state, then the liquid 25 crystal panel 2 does not display a picture. If a state in which the liquid crystal panel 2 does not display a picture upon power-on is sustained, then the liquid crystal is deteriorated to leave traces. Such deteriorated traces is viewed even when the LCD make a normal display to cause a trouble of the LCD.

30

Accordingly, it is an object of the present invention to

provide a liquid crystal display and a driving method thereof that is adapted to display a certain information to a user when no signal is input after a power was applied.

5

In order to achieve these and other objects of the invention, a liquid crystal display device according to one aspect of the present invention includes a liquid crystal display panel having pixel electrodes arranged in a matrix type; a timing controller for generating and outputting control signals for driving the liquid crystal display panel in response to a timing synchronizing signal inputted from the exterior thereof and for re-arranging and outputting an input data; a drive circuit connected between the liquid crystal display panel and the timing controller to display a data inputted from the timing controller on the liquid crystal display panel in response to the control signal; an oscillator for generating a pre-synchronizing signal having a desired frequency to apply the same to the timing controller; a signal presence determiner for comparing the timing synchronizing signal with the pre-synchronizing signal to generate a determining signal indicating an input existence of the timing synchronizing signal; a control signal generator for generating a control signal on the basis of the pre-synchronizing signal in response to a determining signal indicating no input of the timing synchronizing signal; and a data storage device for storing a certain picture data and outputting the picture data to the drive circuit in response to the determining signal indicating no input of the timing synchronizing signal.

A liquid crystal display device according to another

aspect of the present invention includes a liquid crystal display panel having pixel electrodes arranged in a matrix type; an oscillator for generating a reference clock having the same frequency as a horizontal synchronizing signal and a pre-synchronizing signal having the same frequency as a vertical synchronizing signal; a synchronization detector for comparing a data enable signal inputted from the exterior thereof with the reference clock to generate a synchronization-detecting signal indicating an input existence of the reference clock; a signal presence determiner for comparing the synchronization-detecting signal with the pre-synchronizing signal to generate a determining signal indicating an input presence of the data enable signal; a control signal generator for receiving the vertical synchronizing signal inputted from the exterior thereof and the pre-synchronizing signal to generate a control signal on the basis of the pre-synchronizing signal in response to the determining signal when the data enable signal is not inputted; a data storage device for storing a certain picture data and outputting the picture data to a drive circuit in response to the determining signal; and said drive circuit for receiving the picture data inputted from the data storage device to display the same on the liquid crystal panel in response to the control signal.

A method of driving a liquid crystal display device according to still another aspect of the present invention includes the steps of generating a pre-synchronizing signal having a desired frequency by a timing controller; comparing the timing synchronizing signal with the pre-synchronizing signal to generate a determining signal indicating an input existence of a timing synchronizing

signal; generating a control signal on the basis of the pre-synchronizing signal in response to the determining signal indicating no input of the timing synchronizing signal; and outputting a desired picture data to a drive circuit in response to the determining signal.

For a better understanding of the invention, embodiments will now be described, by way of example, with reference to the accompanying drawings, in which:

- Fig. 1 is a block diagram showing a configuration of a general liquid crystal display;
- Fig. 2 is a schematic block diagram showing a configuration of the timing controller in Fig. 1;
- Fig. 3 is a schematic block diagram showing a configuration of a timing controller according to an embodiment of the present invention;
- Fig. 4 is waveform diagrams for showing a generation process of a determining signal generated from the signal presence determiner in Fig. 3;
- Fig. 5 represents a multiplexor installed in the timing controller shown in Fig. 3;
- Fig. 6A is waveform diagrams for showing a generation process of a determining signal generated by another embodiment of the present invention; and
- Fig. 6B is waveform diagrams for showing a process of generating a determining signal using the synchronization-detecting signal in Fig. 6A.

Referring to Fig. 3, there is shown a timing controller according to an embodiment of the present invention. The timing controller 34 includes a control signal generator 30 for receiving timing synchronizing signals, such as a horizontal synchronizing signal, a vertical synchronizing signal, a data enable signal and a clock pulse, etc., from an interface 10 to generate control signals to be applied to a data driver 18 and a gate driver 20, a data signal generator 32 for receiving a data (R,G,B) inputted from the interface 10 to align the same and supplying the aligned data to the data driver 18, a signal presence determiner 28 for monitoring an application state of various control signals inputted from the interface 10, and an oscillator 26 for applying a desired frequency of pre-synchronizing signal to the signal presence determiner 28. The control signal generator 30 receives the horizontal synchronizing signal, the vertical synchronizing signal, the data enable signal and the clock from the interface 10 to generate various control signals for driving the liquid crystal display panel, and applies the generated control signals to the data driver 18 and the gate driver 20. At this time, as an example, the control signal generator 30 generates source sampling clock (SSC), source output enable (SOE), source start pulse (SSP) and liquid crystal polarity inverse (POL) signals, etc. on the basis of the input vertical synchronizing signal to apply the same to the data driver 18. Also, the control signal generator 30 generates gate shift clock (GSC), gate output enable (GOE), gate start pulse (GSP) signals, etc. on the basis of the input vertical synchronizing signal to apply the same to the gate driver 20. Alternatively, the control signal generator 30 may generate the above-mentioned control

signals for driving the liquid crystal display panel on the basis of a data enable signal.

The data signal generator 32 receives a data (R,G,B) from the interface 10 and re-arranges the received data in such a manner to be received to the liquid crystal display panel 2, thereby applying the same to the data driver 18. The oscillator 26 generates a pre-synchronizing signal having the same frequency as the vertical synchronizing signal to apply it to the signal presence determiner 28. The oscillator 26 may be installed at the exterior or the interior of the timing controller 34.

Hereinafter, an operation when there does not exist an input signal from the exterior will be described. First, the signal presence determiner 28 monitors an application of the control signals outputted from the interface 10. An operation process of the signal presence determiner 28 will be described in detail with reference to Fig. 4. Herein, it is assumed that a frequency of the vertical synchronizing signal inputted from the interface 10 is 60Hz, and a signal input presence is determined on the basis of the vertical synchronizing signal in Fig. 4 as an example.

Referring now to Fig. 4, the signal presence determiner 28 receives a vertical synchronizing signal from the interface 10 and, at the same time, receives a pre-synchronizing signal having the same frequency (i.e., 60Hz) as the vertical synchronizing signal from the oscillator 26. The signal presence determiner 28 receiving the vertical synchronizing signal and the pre-synchronizing signal compares the vertical synchronizing

signal with the pre-synchronizing signal in the A region in Fig. 4 supplied with the vertical synchronizing signal to apply a high-state determining signal indicating an effective signal input to the control signal generator 30 if the vertical synchronizing signal is inputted during a desired period (e.g., three periods). The control signal generator 30 supplied with a high-state determining signal receives the vertical synchronizing signal applied from the interface 10. The following operation is identical to a generation operation of a general control signal.

Otherwise, the signal presence determiner 28 compares the vertical synchronizing signal with the pre-synchronizing signal in the B region in Fig. 4 to apply a low-state determining signal to the control signal generator 30 if the vertical synchronizing signal is not inputted during a desired period (e.g., three periods). The control signal generator 30 supplied with the low-state determining signal receives the pre-synchronizing signal from the oscillator 26 to display a full black, a full white or a certain picture information on the liquid crystal display panel 2. To this end, the control signal generator 30 includes a multiplexor (MUX) 40 as shown in Fig. 5. The MUX 40 is supplied with the pre-synchronizing signal, the vertical synchronizing signal and the determining signal, and selects and outputs the pre-synchronizing signal or the vertical synchronizing signal as a synchronizing signal in response to an input state of the determining signal. At this time, if a high-state determining signal is inputted, the MUX 40 selects and outputs the vertical synchronizing signal; whereas, if a low-state determining signal is inputted, the MUX 40 selects and outputs the pre-synchronizing signal. Then, the control signal

generator 30 generates and outputs each control signal on the basis of the vertical synchronizing signal or the pre-synchronizing signal outputted from the MUX 40. The data signal generator 32 has stored, in advance, a data for displaying a certain picture with at least one frame. A ROM used as a storage device may be integrated within a block of the data signal generator 32 in the timing controller 34, or employed by an external flash memory, etc.

10

The data signal generator 32 outputs a certain data stored in advance when a low-state determining signal is inputted, in response to an input state of the determining signal. In this case, a black data or a text data indicating a signal no-input state, etc. is used as the certain data.

In another embodiment of the present invention, a data enable signal may be used to determine a presence of the control signal applied from the interface 10 to the timing controller 34. Referring to Fig. 6A, the signal presence determiner 28 receives a data enable signal from the interface 10 and a detection signal having the same frequency as the horizontal synchronizing signal from the oscillator 26. The signal presence determiner 28 receiving the data enable signal and the detection signal compares the detection signal with the data enable signal to generate a synchronization-detecting signal indicating the detected result. Referring to Fig. 6B, the signal presence determiner 28 receives a pre-synchronizing signal having the same frequency as the vertical synchronizing signal from the oscillator 26 to compare it with the synchronization-detecting signal. The signal presence determiner 28 compares the synchronization-detecting

signal with the pre-synchronizing signal to apply a low-state determining signal to the control signal generator 30 and the data signal generator 32 if the synchronization-detecting signal shows a state that fails 5 to detect an input of the data enable signal during a desired period (e.g., three periods). The control signal generator 30 and the data signal generator 32 supplied with the low-state determining signal receives a pre-synchronizing signal from the oscillator 26 to display a 10 full black, a full white or a certain information on the liquid crystal display panel 2.

As described above, according to the present invention, the timing controller further includes a signal presence 15 determiner to monitor an existence of the control signal inputted from the interface. Accordingly, when a control signal is not inputted from the interface, any one of a certain user information, a full black and a full white 20 can be displayed on the liquid crystal panel to prevent a deterioration of the liquid crystal.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the 25 art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their 30 equivalents.

**CLAIMS:**

1. A liquid crystal display device, comprising:

5 a liquid crystal display panel having pixel electrodes arranged in a matrix type;

a timing controller for generating and outputting control signals for driving the liquid crystal display panel in response to a timing synchronizing signal inputted from the exterior thereof and for re-arranging 10 and outputting an input data;

a drive circuit connected between the liquid crystal display panel and the timing controller to display a data inputted from the timing controller on the liquid crystal display panel in response to the control signal;

15 an oscillator for generating a pre-synchronizing signal having a desired frequency to apply the same to the timing controller;

a signal presence determiner for comparing the timing synchronizing signal with the pre-synchronizing signal to 20 generate a determining signal indicating an input existence of the timing synchronizing signal;

a control signal generator for generating a control signal on the basis of the pre-synchronizing signal in response to a determining signal indicating no input of 25 the timing synchronizing signal; and

a data storage device for storing a certain picture data and outputting the picture data to the drive circuit in response to the determining signal indicating no input of the timing synchronizing signal.

30

2. The liquid crystal display device as claimed in claim 1, wherein the timing synchronizing signal is a vertical synchronizing signal, and the pre-synchronizing signal has

the same frequency as the vertical synchronizing signal.

3. The liquid crystal display device as claimed in claim 1 or 2, wherein, the signal presence determiner generates a determining signal indicating no input state of the vertical synchronizing signal when the vertical synchronizing signal is not inputted identically during three periods of the pre-synchronizing signal.

10 4. The liquid crystal display device as claimed in claim 1, 2 or 3, wherein the control signal generator includes a selector for receiving the timing synchronizing signal and the pre-synchronizing signal to output any one of the two synchronizing signals in response to the determining signal, thereby generating a control signal on the basis of a synchronizing signal outputted from the selector.

15 5. A liquid crystal display device, comprising:  
a liquid crystal display panel having pixel electrodes arranged in a matrix type;  
an oscillator for generating a reference clock having the same frequency as a horizontal synchronizing signal and a pre-synchronizing signal having the same frequency as a vertical synchronizing signal;  
20 a synchronization detector for comparing a data enable signal inputted from the exterior thereof with the reference clock to generate a synchronization-detecting signal indicating an input existence of the reference clock;  
25 a signal presence determiner for comparing the synchronization-detecting signal with the pre-synchronizing signal to generate a determining signal indicating an input presence of the data enable signal;

5 a control signal generator for receiving the vertical synchronizing signal inputted from the exterior thereof and the pre-synchronizing signal to generate a control signal on the basis of the pre-synchronizing signal in response to the determining signal when the data enable signal is not inputted;

10 a data storage device for storing a certain picture data and outputting the picture data to a drive circuit in response to the determining signal; and

15 said drive circuit for receiving the picture data inputted from the data storage device to display the same on the liquid crystal panel in response to the control signal.

20 6. The liquid crystal display device as claimed in claim 5, wherein the signal presence determiner generates a determining signal indicating no input state of the data enable signal when the data enable signal is not inputted during three periods of the pre-synchronizing signal.

25 7. The liquid crystal display device as claimed in claim 5 or 6, wherein the control signal generator includes a selector for receiving the timing synchronizing signal and the pre-synchronizing signal to output any one of the two synchronizing signals in response to the determining signal, thereby generating a control signal on the basis of the synchronizing signal outputted from the selector.

30 8. A method of driving a liquid crystal display device including a liquid crystal display panel having pixel electrodes arranged in a matrix type, a timing controller for generating and outputting control signals for driving the liquid crystal display panel in response to a timing

synchronizing signal inputted from the exterior thereof and for re-arranging and outputting an input data, and a drive circuit connected between the liquid crystal display panel and the timing controller to display a data inputted 5 from the timing controller on the liquid crystal display panel in response to the control signal, said method comprising the steps of:

generating a pre-synchronizing signal having a desired frequency by the timing controller;

10 comparing the timing synchronizing signal with the pre-synchronizing signal to generate a determining signal indicating an input existence of the timing synchronizing signal;

15 generating a control signal on the basis of the pre-synchronizing signal in response to the determining signal indicating no input of the timing synchronizing signal; and

outputting a desired picture data to the drive circuit in response to the determining signal.

20 9. Apparatus for driving a liquid crystal display, including means for detecting a driving signal and means for causing a predetermined output to be displayed when said detecting means does not detect for a given time period an effective driving signal while power is applied to the liquid crystal display.

10. A liquid crystal display device or apparatus substantially as hereinbefore described with reference to and/or substantially as illustrated in any one of or any combination of Figs. 3 to 6B of the accompanying drawings.



INVESTOR IN PEOPLE

Application No: GB 0112233.2  
Claims searched: All

Examiner: Helen Edwards  
Date of search: 18 February 2002

Patents Act 1977  
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed. T): G5C: CHBH, CHBM

Int Cl (Ed.7): G09G: 3/36

Other: Online database: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	US 6069619	(SAMSUNG ELECTRONICS) See figures 1 and 4 and column 3 line 28 to column 6 line 45	1, 8, 9
X	US 5757365	(SEIKO EPSON CO) See column 2 lines 7 to 57	1, 8, 9
X	JP 10319916 A	(MATSUSHITA ELECTRIC) See figure 1 and English abstract	9
X	JP 9191435 A	(SHARP KK) See English abstract	9

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

This Page Blank (uspto)